IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

# APPLICATION FOR LETTERS PATENT

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# CIRCUITRY COMPRISING ROUGHENED PLATINUM LAYERS, PLATINUM-CONTAINING MATERIALS, CAPACITORS COMPRISING ROUGHENED PLATINUM LAYERS, METHODS OF FORMING ROUGHENED LAYERS OF PLATINUM, AND METHODS OF FORMING CAPACITORS

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# CIRCUITRY COMPRISING ROUGHENED PLATINUM LAYERS, PLATINUM-CONTAINING MATERIALS CAPACITORS COMPRISING ROUGHENED PLATINUM LAYERS, METHODS OF FORMING ROUGHENED LAYERS OF PLATINUM, AND METHODS OF FORMING CAPACITORS

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## TECHNICAL FIELD

The invention pertains to methods of forming and using platinum-containing materials, and to circuitry incorporating roughened layers of platinum.

## BACKGROUND OF THE INVENTION

Platinum is a candidate for utilization as a conductive material in advanced semiconductor processing. Platinum can be utilized in an elemental form, or as an alloy (such as, for example, rhodium/platinum), and can be deposited onto a substrate by, for example, sputter deposition or chemical vapor deposition (CVD) methods. Platinum is typically formed to have a relatively smooth upper surface. Such smooth upper surface can be advantageous in, for example, applications in which circuitry is formed over the platinum layer. Specifically, the relatively smooth surface can provide a substantially planar platform upon which other circuitry is formed. However, there can be advantages to incorporating roughened conductive layers into integrated circuitry in applications where high surface area is desired, as with capacitor

electrodes. Accordingly, it would be desirable to develop methods of forming platinum layers having roughened outer surfaces.

In another aspect of the prior art, platinum-comprising materials are frequently utilized as catalysts in, for example, the petroleum industry, as well as in, for example, automobile exhaust systems. Frequently, an efficiency of a catalyst can be improved by enhancing a surface area of the catalyst. Accordingly, it would be desirable to develop methods of enhancing surface area of platinum-comprising materials.

## SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming a roughened layer of platinum. A substrate is provided within a reaction chamber. An oxidizing gas is flowed into the reaction chamber, and a platinum precursor is flowed into the chamber. Platinum is deposited from the platinum precursor over the substrate in the presence of the oxidizing gas. A temperature within the chamber is maintained at from about 0°C to less than 300°C during the depositing.

In another aspect, the invention encompasses a circuit comprising a roughened platinum layer over a substrate. The roughened platinum layer has a continuous surface characterized by columnar pedestals.

In yet another aspect, the invention encompasses a platinum catalyst characterized by a continuous outer surface portion of the platinum having a plurality of columnar pedestals that are at least about 400Å tall. The surface portion covers an area that is at least about 4 x $10^6$ square Angstroms.

## BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic, fragmentary, cross-sectional view of a semiconductive wafer fragment processed according to a method of the present invention.

Fig. 2 is a fragmentary top view of the semiconductor wafer fragment of Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that of Fig. 1.

Fig. 4 is a scanning electron microscope (SEM) micrograph of a platinum film produced by CVD of $MeCpPt(Me)_3$.

Fig. 5 is a SEM micrograph of a platinum film produced by CVD of $MeCpPt(Me)_3$ under different conditions than those utilized for forming the film of Fig. 4.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

The invention encompasses methods of forming platinum layers having roughened outer surfaces, and methods of incorporating such layers into capacitor constructions. Fig. 1 shows a semiconductor wafer fragment 10 at a preliminary processing step of the present invention. Wafer fragment 10 comprises a substrate 12. Substrate 12 can comprise, for example, a monocrystalline silicon wafer lightly doped with a background p-type dopant. To aid in interpretation of the claims that follow, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited

to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

A diffusion region 14 is formed within substrate 12 and defines a node location to which electrical connection with a storage node of a capacitor is to be made. Diffusion region 14 can be formed by, for example, implanting a conductivity enhancing dopant into substrate 12.

An adhesion layer 16 is formed over substrate 12 and in electrical contact with diffusion region 14, and a platinum-comprising layer 18 is formed over adhesion layer 16. Adhesion layer 16 is provided to enhance adhesion of platinum-comprising layer 18 to substrate 12. In other embodiments (not shown) a platinum-comprising layer can be provided directly onto a silicon surface (either the monocrystalline silicon surface of substrate 12, or an intervening amorphous or polycrystalline surface). Such embodiments are less preferred than the shown embodiment due to difficulties of adequately adhering platinum directly to silicon.

Adhesion layer 16 can comprise, for example, at least one of titanium nitride, iridium, rhodium, ruthenium, platinum, palladium, osmium, silver, rhodium/platinum alloy, $IrO_2$, $RuO_2$, $RhO_2$, or $OsO_2$.

Adhesion layer 16 can be formed by, for example, chemical vapor deposition, and can be formed to a thickness of, for example, less than 100Å.

Platinum-comprising layer 18 can comprise, for example, elemental platinum, or a platinum alloy, such as rhodium/platinum alloy. Platinum-comprising layer 18 is provided to have a roughened outer surface 20. Such can be accomplished by chemical vapor deposition of platinum-comprising layer 18 under relatively low temperature conditions, and in the presence of an oxidizing atmosphere. For instance, a platinum-comprising layer 18 formed as follows will comprise a roughened outer surface 20.

First, substrate 12 is inserted within a CVD reaction chamber. An oxidizing gas and a platinum precursor are flowed into the reaction chamber. Platinum is deposited from the platinum precursor over substrate 12 in the presence of the oxidizing gas. A temperature within the reaction chamber is maintained at from about 0°C to less than 300°C during the depositing, and a pressure within the reactor is preferably maintained at from about 0.5 Torr to about 20 Torr. Suitable control of the temperature and of a relative flow rate of the oxidizing gas to the platinum precursor causes deposited platinum layer 18 to have a roughened outer surface 20. The platinum precursor is flowed into the reaction chamber in a carrier gas, such as, for example, a gas known to be generally inert to reaction with platinum precursor materials, such

as, for example, helium or argon. The platinum precursor can comprise, for example, at least one of $MeCpPtMe_3$, $CpPtMe_3$, $Pt(acetylacetonate)_2$, $Pt(PF_3)_4$, $Pt(CO)_2Cl_2$, cis-$[PtMe_2(MeNC)_2]$, or platinum hexafluoroacetylacetonate; wherein Cp is a cyclopentadienyl group and Me is a methyl group. The oxidizing gas can comprise, for example, at least one of $O_2$, $N_2O$, $SO_3$, $O_3$, $H_2O_2$, or $NO_x$, wherein x has a value of from 1 to 3. In embodiments wherein platinum layer 18 comprises a platinum/metal alloy, at least one other metal precursor can be flowed into the reaction chamber to deposit the platinum as an alloy of the platinum and the at least one other metal. The at least one other metal precursor can comprise, for example, a precursor of rhodium, iridium, ruthenium, palladium, osmium, and/or silver.

The oxidizing gas can assist in deposition of platinum from the platinum-comprising precursor by oxidizing carbon from the precursor during deposition of the platinum. Also, the oxidizing gas can influence a deposition rate of a platinum-comprising layer. Specifically, a greater rate of flow of the oxidizing gas relative to the flow of the platinum precursor can lead to faster deposition of the platinum-comprising layer. The rate of flow of platinum precursor is influenced by a rate of flow of carrier gas through a liquid organic precursor solution, and by a temperature of the precursor solution. In preferred embodiments of the invention, a carrier gas will be flowed through a liquid organic precursor solution at a rate of from about 2 sccm to about 1000 sccm and more

preferably at less than or equal to about 30 sccm. In such preferred embodiments, the oxidizing gas will be flowed at a flow rate of at least about 50 sccm. The organic precursor will preferably be at a temperature of from about 0°C to about 100°C, and more preferably from about 30°C to about 50°C.

A rate of growth of platinum-comprising layer within the reaction chamber is also influenced by a temperature of the substrate. Specifically, if platinum is deposited under conditions wherein the temperature of the substrate is maintained at from about 220°C to less than 300°C, the platinum will deposit at a rate of about 600Å in about 30 seconds. If a temperature of the substrate is reduced to below about 210°C, a rate of deposition of platinum will decrease considerably. It is preferred that a deposition time for a 600Å thick platinum-comprising layer be less than or equal to about 40 seconds to maintain efficiency of a production process. Accordingly, it is preferred that the temperature of the substrate be maintained at above about 210°C, and preferably at from greater than or equal to about 220°C during deposition of the platinum-comprising layer within the reaction chamber.

It is also found that if a temperature is greater than 300°C and less than about 350°C, a deposited platinum layer will have a smooth outer surface, rather than a desired roughened outer surface. Further, if the temperature of the substrate exceeds about 400°C, a deposited platinum surface will have holes extending to a surface underlying the

platinum surface, rather than being a continuous surface overlying a substrate. Accordingly, it is preferred that the temperature of the substrate be well below 400°C, more preferred that the temperature be below 300°C, and even more preferred that the temperature be less than or equal to about 280°C. In preferred embodiments of the present invention, the temperature of the substrate will be maintained at from about 220°C to about 280°C, whereupon it is found that a platinum layer having a roughened outer surface can be deposited to a thickness of about 600Å in about 30 seconds.

Platinum layer 18 is preferably deposited to a thickness of at least about 400Å to avoid having surface anomalies (such as crevices or holes) that extend entirely through layer 18 to an underlying layer, and is preferably deposited to a thickness of at least about 600Å. However, in some embodiments holes extending entirely through layer 18 will be of little or no consequence in semiconductor circuitry ultimately formed from layer 18. Such embodiments can include, for example, embodiments wherein adhesion layer 16 is provided beneath platinum-comprising layer 18. Accordingly, in embodiments wherein platinum layer 18 is provided over an adhesion layer 16, it can be preferred to provide platinum layer 18 to a thickness of less than 400Å because of space limitations due to the close packing of capacitors. Also, in embodiments in which platinum layer 18 is utilized in forming circuitry having tight spacing requirements it can be preferred to form layer 18 to be

relatively thin. For instance, in some capacitor constructions it can be desired to form layer 18 to be less than or equal to about 1000Å, and more preferred to form layer 18 to be from about 300Å to about 400Å to avoid electrical contact between adjacent capacitor structures.

A fragmentary top view of wafer fragment 10 is shown in Fig. 2. Layer 18 is preferably a continuous layer (defined as a layer without cavities extending therethrough to an underlying layer -- such as the underlying layer 16 of Fig. 2) across its entirety. Alternatively, some portion of layer 18 is continuous. For example, consider an application where layer 18 overlies and contacts a conductive layer to form a circuit device comprising both layer 18 and the underlying conductive layer. In such applications, it is generally still desired that a substantial portion of layer 18 be continuous to, for example, maintain a uniform electrical contact between layer 18 and the underlying conductive layer. Such substantial portion will preferably cover a surface area of at least about $4 \times 10^6$ square Angstroms. A surface area of about $4 \times 10^6$ square Angstroms is illustrated in Fig. 3 as a square 50 having sides of about 2000 Angstroms.

Fig. 3 illustrates an embodiment wherein platinum-comprising layer 18 is incorporated into a capacitor construction 30 as a storage node. Specifically, a dielectric layer 22 and a capacitor electrode 24 are provided over platinum-comprising layer 18 to form capacitor construction 30. Dielectric layer 22 can comprise one or more of silicon

oxide or silicon nitride, or it can comprise other dielectric materials, such as, for example, tantalum pentoxide, or $BaSrTiO_3$. Capacitor electrode 24 can comprise, for example, TiN, conductively doped silicon (such as polysilicon), or a metal, such as, for example, platinum. In embodiments wherein capacitor electrode 24 comprises platinum, capacitor electrode 24 can be formed by chemical vapor deposition over dielectric layer 22. The chemical vapor deposition can be conducted either to form upper electrode 24 with a relatively smooth upper surface, or to form upper electrode 24 with a relatively rough upper surface. If capacitor electrode 24 is to be formed of platinum with a relatively smooth upper surface, it can be chemical vapor deposited in a reaction chamber with a temperature maintained at above about 300° C and/or with an oxidizing gas flow rate of less than 50 sccm and a carrier gas flow rate of greater than 30 sccm. Also, any platinum comprised by capacitor electrode 24 can be in the form of elemental platinum, or an alloy, such as, for example, rhodium/platinum alloy.

As shown, layer 18 has a rough outer surface and layers 22 and 24 are conformal to the rough outer surface of layer 18.

Figs. 4 and 5 illustrate scanning electron microscope (SEM) micrographs of platinum films produced by CVD of $MeCpPt(Me)_3$. Fig. 4 illustrates a surface produced within a reaction chamber in a time of about 6 minutes, wherein a temperature in the chamber was about 215°C, a pressure was about 5 Torr, a flow rate of carrier gas

(He, with a pressure at the carrier gas bubbler of about 6 Torr) was about 5 sccm, and a flow rate of oxidizing gas ($O_2$) was about 50 sccm. The platinum surface formed comprises pedestals characteristic of columnar growth. The columnar pedestals terminate in dome-shaped (substantially hemispherical) tops. It can be advantageous to have substantially hemispherical tops, rather than tops having sharp edges, in forming capacitor constructions or other electronic circuitry from a deposited platinum layer. Specifically, the relatively rounded hemispherical surfaces can create relatively uniform electric fields at the surface of a deposited platinum layer. In contrast, if sharp edges were present, the sharp edges could form loci for high electric fields, and lead to leakage of electric current across the capacitor. The platinum layer illustrated in Fig. 4 can be referred to as "hemispherical grain" platinum to indicate a structure largely analogous to a material known in the art as hemispherical grain polysilicon.

The platinum layer of Fig. 4 is characterized by columnar pedestals generally having heights greater than or equal to about one-third of a total thickness of the platinum layer. Many of the pedestals shown in Fig. 4 have a height approximately equal to a thickness of the deposited platinum layer. Accordingly, if the deposited platinum layer has a thickness of about 600Å, the individual pedestals can have a thickness approaching 600Å. Such is only an approximation to the size of the pedestals as it is found that some of the pedestals will grow from

surfaces of other pedestals, and some of the pedestals will grow less vertically than other pedestals. An average diameter of the pedestals is about 200Å, and the pedestals are generally closely packed (i.e., the pedestals generally touch other pedestals and many pedestals fuse with other pedestals), but the distribution of the pedestals is typically not a close-packed structure (i.e., a structure wherein all the pedestals are tightly packed in, for example, an hexagonal type arrangement to form a maximum number of pedestals on a given surface). The columnar growth illustrated in Fig. 4 is found not to occur if a temperature within a CVD reaction chamber is above 300°C.

Fig. 5 illustrates a surface produced on a platinum film within a reaction chamber in a time of about 150 seconds, wherein a temperature in the chamber was 300°C, a pressure was about 0.5 Torr, a flow rate of carrier gas (He, with a pressure at the carrier gas bubbler of about 6 Torr) was about 30 sccm, and a flow rate of oxidizing gas ($O_2$) was about 10 sccm. The platinum layer deposited under the Fig. 5 conditions has a much smoother surface than that deposited under the Fig. 4 conditions. Figs 4 and 5 together evidence that it is possible to control a grain structure of a surface of a chemical vapor deposited platinum layer by controlling process parameters of a chemical vapor deposition reaction chamber.

Although the invention has been described with application to formation of a capacitor structure, it is to be understood that the

invention can be utilized in a number of other applications as well. For instance, a platinum layer having a roughened surface can be utilized for formation of catalysts.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.